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Application of HfO_2 high-k gate insulator for excimer laser annealed poly-Si TFT

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Abstract The electrical characteristics of polycrystalline silicon (poly-Si) thin film transistor (TFT) crystallized by excimer laser annealing (ELA) method with high-k gate dielectrics were evaluated. Because a high thermal budget is inevitable for conventional fabricating process of poly-Si TFTs, an amorphous silicon film on a buried oxide was crystallized by annealing with a KrF excimer laser (248) to fabricate a poly-Si film at low temperature. Furthermore, the high permittivity HfO_2 film with a thickness of 20 nm as the gate-insulator was deposited by atomic layer deposition (ALD) to low temperature process. In addition, the solid phase crystallization (SPC) was compared to the ELA method as a crystallization technique of amorphous-silicon film. As a result, the crystallinity and surface roughness of poly-Si crystallized by ELA method was superior to the SPC method. Also, we obtained excellent device characteristics from the poly-Si TFT fabricated by the ELA crystallization method.

Keywords Poly-Si TFT · Excimer laser anneal · Solid phase crystallization · High-k · HfO_2

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1 Introduction

The number of transistors per unit area is increased by Moore's scaling law up to 2004. And the line widths of transistor historically have shrunk every 3 years, and recently line widths have been shrinking every 2 years at the same time. Conventional bulk MOSFETs had the problems of short channel effect such as leakage current and subthreshold properties degradation due to the reduction of devices and physical limitation. In order to solve these problems, the device technology has suggested the thin film formed on after growth the insulator on the substrate. The poly-Si TFT has the advantages of stacked device structure, large area process and simple fabrication process. Also, the polycrystalline silicon thin-film transistor (poly-Si TFT) has higher electric field-effect-mobility and larger drivability than the amorphous silicon TFT [1]. So, it is expected to be the next generation ultra large-scale integration (ULSI) device technology which can improve the degree of integration and the performance of circuit, because the realization of three-dimensional integrated circuit, which is impossible to realize by using the conventional bulk silicon process, is possible [2–4]. Many researches have been accomplished on the manufacturing of poly-Si film at low temperature; particularly the laser crystallization method has attracted much attention to obtain a high quality poly-Si film at low temperature [5, 6].

As the thickness of conventional SiO_2 as the gate dielectrics in MOSFETs shrinks below ~2 nm, large leakage current and reliability concerns dictate the search for new dielectric materials for the gate stack with permittivity higher than that of SiO_2 [7–9]. These high-k gate dielectrics are expected as the novel materials to overcome the limitation of SiO_2.

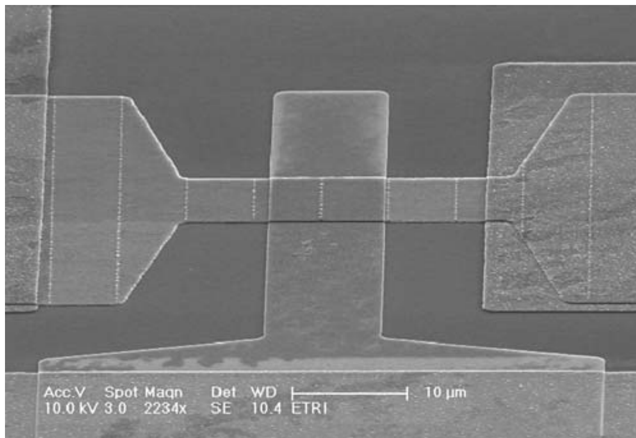

Fig. 1 SEM image of fabricated poly-Si TFT

In this paper, we investigated the electrical characteristics of polycrystalline silicon (poly-Si) thin film transistor (TFT) crystallized by excimer laser annealing (ELA) method with high-k gate dielectrics of hafnium dioxide.

2 Experimental

The thermal oxide with a thickness of 200 nm was grown on the (100) *p*-type bulk silicon wafer. The amorphous silicon film with a thickness of 100 nm was deposited on the thermal oxide by low pressure chemical vapor deposition (LPCVD) method at 550°C. The crystallization of amorphous silicon film was carried out in vacuum chamber at 300 mTorr using the KrF excimer laser of 248 nm wavelength. The crystallization process temperature was maintained at 20°C. The energy density optimized 400 mJ/cm^2. For comparison, the SPC method as crystallization method of amorphous silicon film was carried out. The amorphous silicon films were crystallized by annealing at 600°C for 24 h in a conventional furnace with N_2 ambient. The crystallinity, grain size and surface roughness of crystallized poly-Si films were analyzed by X-ray diffractometer (XRD) and scanning electron microscope (SEM), respectively. The poly-Si active region was defined by photolithography and etching processes. Then, HfO_2 as the gate insulator with a thickness of 20 nm was formed by atomic layer deposition (ALD) and the aluminum with a thickness of 200 nm was deposited on the gate insulator by thermal evaporator. After definition of gate electrode by photolithography and etching, the doping of source/drain region was followed using elevated temperature doping at 450°C which can achieve the doping and activation of an impurity simultaneously [10]. Figure 1 shows the SEM image of fabricated poly-Si TFT.

3 Results and discussion

Figure 2 shows the SEM images of poly-Si films after etching of the grain boundary by Secco etchant. Since the SPC induces the self-crystallization of amorphous silicon films using the high temperature annealing of 600°C, the poly-Si films by SPC method have small grains and wide grain boundary as shown in Fig. 2(b). On the other hand, the larger silicon grains were obtained by ELA crystallization method. As shown in Fig. 2(a), the clearer and narrower grain boundaries are also observed. Additionally, the poly-Si film by ELA method had very smooth surface. As a result of AFM analysis, the RMS roughness of poly-Si film crystallized by ELA method was 1.6 nm. Therefore, we can conclude that the fabrication of TFT device by ELA crystallization method is more desirable, because the surface roughness of poly-Si film resulted in the mobility degradation of TFT and early breakdown of gate insulator.

Figure 3 shows XRD intensity profiles of films after SPC and ELA methods. The XRD patterns shown in this figure are the optimized conditions for both crystallization

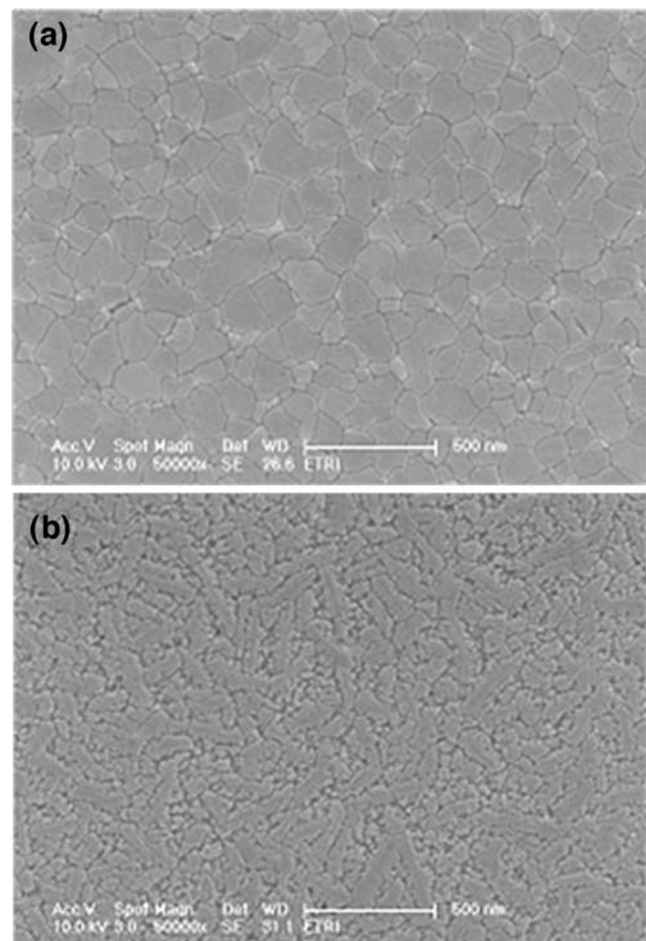

Fig. 2 SEM images of poly-Si films after Secco etching of grain boundary; (**a**) ELA (400 mJ/cm^2), (**b**) SPC (600°C, 24 h)

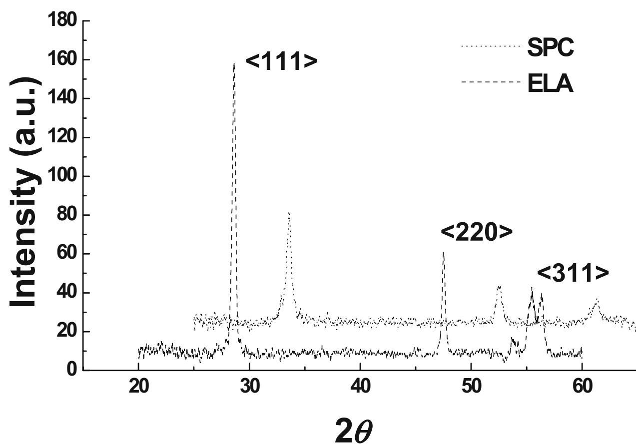

Fig. 3 Results of XRD analysis obtained from poly-Si films. ELA (400 mJ/cm^2), SPC (600°C, 24 h)

methods. The preferred crystal orientations of poly-Si films are irrelevant to the crystallization method and all the poly-Si films revealed (111), (220) and (311) direction peaks; particularly a strong diffraction occurred at (111) crystal plane. The intensity of XRD obtained from the ELA method was stronger than that from the SPC method. Therefore, it is concluded that the crystallinity of ELA crystallized poly-Si is superior to that of the SPC Poly-Si.

Figure 4 shows the I_D-V_G characteristics of the poly-Si TFTs with channel width/gate length, W/L=20 um/10 um fabricated by SPC and ELA crystallization methods. In the poly-Si TFT by SPC and ELA methods as shown in Fig. 4, the subthreshold swing (SS) was estimated 214.2 mV/dec and 161.1 mV/dec, respectively. As shown in Figs. 2 and 3, the poly-Si TFT crystallized by the ELA method showed the electrical characteristics more excellent than that by the SPC. Additionally, the poly-Si TFTs with HfO_2 as the gate insulator crystallized by the ELA and SPC methods can be improved by the post-annealing because of the trap existed at the interface between the silicon and HfO_2.

Figure 5 shows the I_D-V_D characteristics of poly-Si TFT with channel width/gate length, W/L=20 um/10 um fabricated by ELA crystallization methods. In the poly-Si TFT by SPC and ELA as shown in Fig. 5, the saturation drain current ($I_{D,sat}$) was estimated 1.26×10^{-6} A and 2.46×10^{-6} A, respectively. The poly-Si TFT crystallized by ELA method was slightly improved than that by the SPC method. A further improvement of drain saturation current and carrier mobility can be achieved by applying the metal-silicide at source/drain region, because the poly-Si TFT fabricated in this work has large parasitic resistance components at source/drain region. Based on these results, the excimer laser crystallization method used is considered to be valuable for the large area device fabrications, because the excimer laser source used in this work has a large beam area of 1.1×55 mm^2.

4 Conclusion

The poly-Si TFT having low temperature process for the application of high performance 3D CMOS devices was achieved by ELA method and HfO_2 as the gate insulator. The poly-Si TFT with HfO_2 was obtained the acceptable characteristics. But, the poly-Si TFT with HfO_2 has still the problems of high interface trap density, surface roughness and weak thermal stability. So, the laser-annealing and post-annealing processes are required to overcome these problems. We can conclude that HfO_2 as gate insulator is expected as the replaced of the conventional silicon oxide materials. Also, the ELA crystallization method developed in this work is very effective for the fabrication of high integrated 3D ULSI circuits and future display devices.

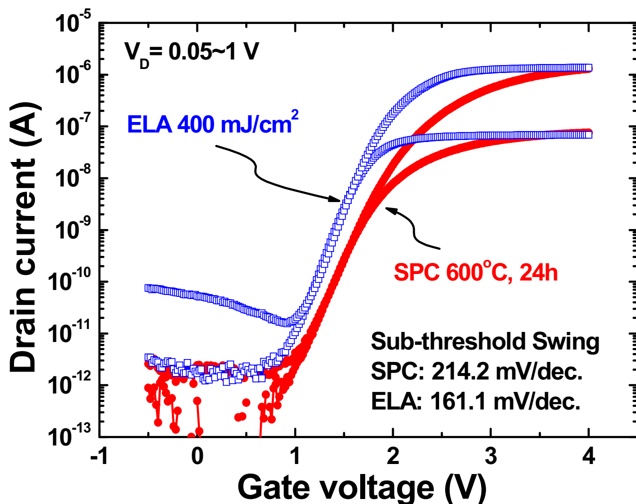

Fig. 4 I_D-V_G characteristics of poly-Si TFT fabricated by ELA (400 mJ/cm^2), SPC (600°C, 24 h)

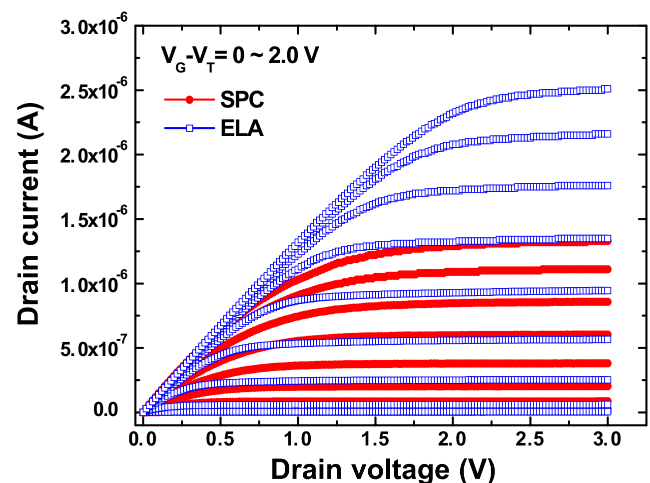

Fig. 5 I_D-V_D characteristics of poly-Si TFT fabricated by ELA (400 mJ/cm^2), SPC (600°C, 24 h)

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